REMARKS

In the Office Action dated March 4, 2003, the Examiner rejected claim 1 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,920,084; rejected claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Wakai et al. (USP 5,003,356), in view of Hughes et al. (USP 5,591,676).

In the Amendment filed September 3, 2003, Applicant canceled claim 1 and added new claims 23-32. In the Office Action dated November 7, 2003, the Examiner stated that the reply filed on September 3, 2003 is not fully response to the March 4, 2003 Office Action because new claims 23-32 are drawn to a new and independent invention.

In response, Applicant cancels claims 23-32 and presents new claims 33-42.

Claims 33-36 are allowable over the cited references in that these claims recite a combination of features including, for example, an array of substantially transparent pixel electrodes on the substrate over the insulating layer so that the patterned pixel electrodes overlap the gate and drain lines in order to increase a pixel aperture ratio of the display, wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes with one of the gate and drain lines is no greater than 0.01pF. None of the cited references, singly or combined, teaches or suggests at least these features of the present invention.

Claims 37 and 38 are allowable over the cited references in that these claims recite a combination of features including, for example, an array of substantially transparent pixel electrodes on the substrate over the insulating layer so that the pixel electrodes overlap the address lines in order to increase a pixel aperture ratio of the display, wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes with one of the address lines is no greater than 0.01pF. None of the cited references, singly or combined, teaches or suggests at least these features of the present invention.

Claims 39-42 are allowable over the cited references in that these claims recite a combination of features including, for example, an array of pixel electrodes over the insulating layer and overlapping the gate and drain address lines, wherein a parasitic capacitance corresponding to an overlap of one of the pixel electrodes with one of the gate and drain address lines is no greater than 0.01pF. None of the cited references, singly or combined, teaches or suggests at least these features of the present invention.

Therefore, Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

Should the Examiner deem that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at 202 496-7413.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: May 7, 2004

Respectfully submitted,

By_____

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